REMARKS

Introduction

This Reply is in response to the Office Action of March 8, 2005. Reconsideration of this application in view of the following remarks is respectfully requested.

In the Office Action, claims 20 and 21 were withdrawn from consideration as being directed to a non-elected invention.

Claims 1-8, 10, 11, 13, 16-19, 22, and 30-36 were rejected under 35 U.S.C. §102(e) as being anticipated by Kothandaraman U.S. Patent 6,624,499 ("Kothandaraman"). Claims 9 and 12 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kothandaraman in view of an unspecified "remark." These rejections are respectfully traversed.

Claims 1-7, 9-13, and 16-19

Claims 9 and 12 were rejected under 35 U.S.C. §103(a).

Applicants' invention relates to electrically-programmable integrated circuit fuses. With one aspect of applicants' invention, heat sinks are used to create temperature gradients. FIG. 5 shows a heat sink arrangement in which a heat sink is used at each end of a fuse link. FIGS. 6 and 7 show illustrative heat sink arrangements in which a heat sink is provided in the middle of the fuse link as well as at both ends.

The temperature profiles that are produced in the fuse link when using various heat sink arrangements are shown in FIG. 8.

As shown in FIG. 8, when a heat sink is provided at both ends of a link, as with structures of the type shown in FIG. 5, the link may develop a thermal profile with significant gradients, such as thermal profile 98. As shown by the downward-sloping ends of profile 98, the temperature of the link in the vicinity of heat sinks is less than the temperature in the center of the link.

When a heat sink arrangement of the type shown in FIG. 7 or FIG. 8 is used, the fuse link may develop a thermal profile along its longitudinal axis such as profile 100 of FIG. 8. Central region 101 of profile 100 exhibits a temperature reduction due to the use of the middle heat sink.

The thermal gradients that are established in the fuse link as a result of using the heat sinks help to blow the link during programming.

Original claim 8 was directed to a heat sink arrangement in which heat sinks are located at either end of the fuse link (i.e., there is one heat sink at one end of the link and another heat sink at the other end of the link). Claim 1 has been amended to incorporate the features of original claim 8. An advantage of this type of heat sink arrangement is that

it produces temperature profiles such as profile 98 of FIG. 8, which help blow the fuse link during programming.

In the Office Action, it was suggested that column 4, lines 25-38 and FIG. 8A of Kothandaraman disclosed applicants' two-heat-sink feature. Applicants disagree.

At column 4, lines 25-38 of Kothandaraman, Kothandaraman discusses the single heat sink arrangement of FIG. 8A. In this arrangement, a metal layer 401 is coupled in a "heat transfer relationship" to one end of Kothandaraman's fuse link 106 (i.e., the cathode end 104). There is no comparable metal layer at the other end of link 106. As clearly shown in the top view of the fuse link 106 in FIG. 8A, the anode end 102 of link 106 has no metal layer for heat transfer. The only metal layer that is used for heat transfer in Kothandaraman is metal layer 401.

Because claim 1 is directed to fuses that have a heat sink at each end of their fuse link portion, whereas Kothandaraman discloses an arrangement having only a single heat sink at one end of its fuse link, claim 1 is not anticipated by Kothandaraman. Claims 2-7, 9-13, and 16-19 depend from claim 1 and are allowable because claim 1 is allowable.

Claims 14, 15, 22-25, and 27-29

Claims 14, 15, and 25-29 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. This has been done as follows:

Claim 14 has been placed in independent form incorporating the features of claim 1, from which claim 14 previously depended.

Claim 15 has been placed in independent form incorporating the features of claim 1, from which claim 15 previously depended.

Claim 25 has been placed in independent form incorporating the features of original claim 22, from which claim 25 previously depended.

The features of allowable claim 26 have been placed into claim 22, from which claim 26 previously depended. Allowable claims 27 and 28 have been amended to ensure that the language of claims 27 and 28 is consistent with the new language of claim 22, from which claims 27 and 28 each depend.

Claim 29 has been placed in independent form incorporating the features of claim 22, from which claim 29 previously depended.

In view of these amendments, independent claims 14, 15, 22, 25, and 29 are in condition for allowance. Claims 23, 24, 27, and 28, are in condition for allowance because they depend from claim 22.

Claims 30 and 33

Claim 30 has been amended to incorporate the features of original claim 36, which has been canceled.

Original claim 36 was directed to a fuse formed on a silicon-on-insulated substrate. In the fuse structure defined by original claim 36, the buried oxide layer in the silicon-on-insulator substrate is adjacent to a semiconductor line that forms the fuse link.

In the Office Action, it was suggested that column 4, lines 13-67, column 5, lines 1-22, and FIG. 8B of Kothandaraman disclose a silicon-on-insulator fuse structure of the type defined by claim 30. Applicants disagree.

In the passage of Kothandaraman at column 4, lines 13-67, Kothandaraman describes the fuse structure shown in FIGS. 8A and 8B. At lines 19 and 20, Kothandaraman states that the anode 102, cathode 104, and fuse link 106 of Kothandaraman's fuse are preferably disposed on a substrate. It is stated that the substrate may be a semiconductor substrate. No mention is made

of using a silicon-on-insulator (SOI) wafer for the semiconductor substrate of Kothandaraman.

The cross-sectional view of FIG. 8B in Kothandaraman shows that Kothandaraman's anode 102, cathode 104, and fuse link 106 are formed on an oxide layer 801 on the surface of silicon layer 803. The substrate 101 is formed from a silicon wafer 803 covered by a conventional surface oxide 801. Substrate 101 is not an SOI wafer and therefore does not have a buried oxide layer.

Because Kothandaraman's substrate 101 is a conventional semiconductor substrate, whereas claim 30 is directed to a fuse formed on an SOI substrate, claim 30 is not anticipated by Kothandaraman and is in condition for allowance. Claim 33 depends on claim 30 and is allowable because claim 30 is allowable.

Conclusion

The foregoing demonstrates that claims 1-7, 9-19, 22-25, 27-30, and 33 are in condition for allowance. This application is therefore in condition for allowance.

Reconsideration and allowance of the application are respectfully requested.

Respectfully submitted,

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